CLAIMS

We claim:

1. A method of forming a transistor comprising:

forming a gate conductor on a top surface of a substrate;

forming spacers on sides on the gate conductor;

providing extension regions in the substrate extending at least under the spacers;

forming diffusion regions in the substrate adjacent to the extension regions;

removing a part of at least one of the spacers to expose a portion of the extension region at the top surface of the substrate;

contacting the exposed portion of the extension region with a metal layer.

2. The method of claim 1 wherein the spacers comprise a permanent portion adjacent to the gate conductor and a disposable portion provided on the permanent portion.

3. The method of claim 2 wherein the permanent portion is nitride and the disposable portion is oxide.

4. The method of claim 2 wherein the removing step removes the disposable portion of the spacer.

5. A method of forming an FET on an SOI substrate, comprising:

providing an SOI substrate having a silicon base substrate, an insulative layer on the base substrate, and a silicon layer on the insulative layer;

forming a conductive gate on the silicon layer;

forming first spacers on sidewalls of the gate and on the silicon layer;

implanting diffusion extensions into the silicon layer adjacent to and extending under the gate;

forming second spacers on the first spacers and on the silicon layer;

implanting deep diffusions into the substrate layer adjacent to the second spacers and abutting the diffusion extensions, wherein the silicon layer between the deep diffusions defines a body region of the FET;

removing the second spacer from at least one of the first spacers on the sidewalls of the gate including exposing a portion of the diffusion extension in the silicon layer under the second spacer; and

forming a metal layer in the silicon layer at least in the exposed portion of the diffusion extension, wherein the metal layer is formed deep enough to contact the diffusion extension.

6. The method of claim 5 wherein the deep diffusions are implanted down to the insulative layer.

7. The method of claim 5 wherein the metal layer is formed deeper into the silicon layer than the diffusion extension.

8. The method of claim 7 wherein the metal layer abuts each of: the exposed portion of the diffusion extension, the body region of the FET, and the deep diffusion that was abutting the diffusion extension.

9. The method of claim 5 wherein the metal layer contacts a dopant concentration of 1e19 or less in the extension region.

10. A method of forming a transistor comprising:

providing an SOI substrate;

forming a gate conductor on the substrate;

forming first spacers on sidewalls of the gate;

forming extension regions in the substrate adjacent to the first spacers;

forming second spacers on the first spacers;

implanting diffusion regions into the substrate adjacent to the second spacers;

removing at least one of the second spacers to expose a portion of the extension region; and

forming a metal layer in the substrate contacting at least the extension region.

11. The method of claim 10 wherein the extension region extends under the gate.

12. The method of clam 10 wherein the second spacers are formed on a portion of the extension region.

13. The method of claim 10 wherein the diffusion regions are formed down to an insulating layer.

14. The method of claim 10 wherein the diffusion regions define a body therebetween.

15. The method of claim 10 wherein the metal layer is also formed in the diffusion regions.

16. The method of claim 14 wherein the metal layer extends through the extension region to contact the body.

17. The method of claim 10 wherein both second spacers are removed.

18. The method of claim 10 wherein the metal layer is formed on both sides of the gate.

19. The method of claim 10 wherein the metal layer is self-aligned to the first spacer.

20. The method of claim 10 wherein the first and second spacers are formed from different materials.

21. The method of claim 20 wherein the first spacers is a nitride and the second spacer is an oxide.

22. The method of claim 20 wherein the removing step comprises:

forming a mask exposing one side of the transistor; and

performing a dip to selectively remove the material of the second spacer.

23. A semiconductor device comprising:

a semiconductor layer formed on an insulating layer;

a gate conductor formed on the semiconductor layer;

spacers formed on sidewalls of the gate conductor and on the semiconductor layer;

extension regions arranged in the semiconductor layer on both sides of the gate conductor and extending at least under the spacers;

diffusion regions formed in the semiconductor material adjacent to the extension regions such that a portion of at least one of the extension regions is exposed at a surface of the semiconductor layer;

a metal layer formed at least in the exposed portion of the extension region.

24. The device according to claim 23 wherein the extension regions are lower doped then the diffusion regions.

25. The device according to claim 23 wherein the metal layer also contacts the diffusion region.

26. ~~The device according to claim~~ 23 wherein the metal layer contacts the semiconductor layer.

27. The device according to claim 23 wherein the extension region is exposed on both sides of the gate conductor and the metal layer is formed in both the exposed portions of the extension regions.

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